



10/628074

C.92

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Moacanin et al.

Attorney Docket No.: FULCP010

Patent: 7,260,753 B2

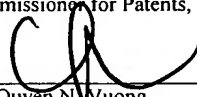
Issued: August 21, 2007

Title: METHODS AND APPARATUS FOR  
PROVIDING TEST ACCESS TO  
ASYNCHRONOUS CIRCUITS AND SYSTEMS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on May 29, 2008 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: \_\_\_\_\_

  
Quyen N. Vuong

**REQUEST FOR CERTIFICATE OF CORRECTION  
OF OFFICE MISTAKE  
(35 U.S.C. §254, 37 CFR §1.322)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
Attn: Certificate of Correction

**Certificate  
JUN 03 2008  
of Correction**

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

**CLAIMS:**

1. In line 7 of claim 20 (column 12, line 39) change "circiut" to --circuit--. This appears correctly in the Amendment as filed on March 27, 2007, on page 8, line 18.

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It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 504480 (Order No. FULCP010).

Respectfully submitted,  
Weaver Austin Villeneuve & Sampson LLP

A handwritten signature in black ink, appearing to read "Joseph M. Villeneuve", followed by a long horizontal flourish.

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asynchronous input data and shifting out the asynchronous output data, an update operation for transmitting the asynchronous input data to the first test register, and a capture operation for receiving the asynchronous output data from the second test register, and ~~The test interface of claim 10~~ wherein the shift register is operable to receive the asynchronous output data in response to a control bit in the asynchronous output data indicating validity of the asynchronous output data.

Please cancel claims 16 and 17 without prejudice.

16-17. (Canceled)

18. (Currently amended) The test interface of claim ~~4~~ 3 wherein the test interface is part of a JTAG compliant interface.

Please cancel claims 19-32 without prejudice.

19-32.(Canceled)

33. (Currently amended) A method for testing an asynchronous circuit using synchronous test equipment, comprising:  
converting synchronous input data received from the synchronous test equipment to asynchronous input data;  
transmitting the asynchronous input data to a first test register in the asynchronous  
circuit;

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(Also Form PT-1050)

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,260,753 B2

DATED : August 21, 2007

Page 1 of 1

INVENTOR(S) : Moacanin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims:**

In line 7 of claim 20, change "circiut" to --circuit--.

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